MICROMACHINED INDUCTORS AND CAPACITORS

JUN ZOU
JACK CHEN
CHANG LIU

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Grainger Center for Electric Machinery and Electromechanics
Department of Electrical and Computer Engineering
University of Illinois at Urbana/Champaign
Urbana, Illinois 61801

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This technical report is a collection of reprints that describe micromachined, integrated passive components including inductors and capacitors. Passive components are important for low power, light weight, integrated power electronics devices such as dc transformers, and also for radio frequency communication devices operating at above 100 MHz. It is critically important to increase the performance of such passive components while realizing integrated microfabrication technologies that allow these components to be fully integrated with power electronics chips or radio-frequency communication chips. The integration allows for lower costs of fabrication and packaging, and for miniaturization of the system.

Novel microfabrication processes were developed for a vertical, out-of-plane inductor, which features a planar coil plane perpendicular to the substrate. This reduces the footprint of the inductor and increases its quality factor by reducing RF leakage loss. The fabrication process is largely compatible with integrated circuit fabrication and therefore can be widely used in IC foundries in the future. A novel architecture was also developed for a planar, parallel-plate capacitor that provides a greater tuning range than conventional micromachined tunable capacitors. It is important for realizing a larger range of system tunability to accommodate different communication protocols.

Research featured in these papers was completed by Dr. Jun Zou and Mr. Jack Chen. Dr. Zou earned his Ph.D. degree in May 2002 and continues to work in a postdoctoral position in Dr. Chang Liu's group and in a collaboration project with Prof. Patrick Chapman. .

Professor Chang Liu, Head
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March 2003

DEVELOPMENT OF THREE-DIMENSIONAL INDUCTORS USING PLASTIC DEFORMATION MAGNETIC ASSEMBLY (PDMA)

Jun Zou[1], Chang Liu, Drew Trainor, Jack Chen, Jose Schutt-Ainé, and Patrick Chapman

Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign
Urbana, IL 61801, USA

Keywords: vertical spiral inductor, on-chip solenoid inductor, 3-D assembly, PDMA

[1] Corresponding author: Jun Zou, 319B Micro and Nanotechnology Laboratory, 208 North Wright Street, Urbana, IL 61801. Phone: 1-217-265-0808. Email: junzou@uiuc.edu.

ABSTRACT

On-chip inductors are critical for enabling portable, power-efficient wireless communication systems. Existing on-chip spiral inductors based on conventional planar IC (integrated circuit) fabrication technology suffer from substrate loss and parasitics, and have relatively large footprints. In this paper, we discuss the development of two types of on-chip 3-D (three-dimensional) inductors – a vertical spiral inductor and a solenoid inductor, by using a 3-D assembly process called plastic deformation magnetic assembly (PDMA). Prototype vertical spiral inductors and solenoid inductors have been fabricated and tested. Experimental results show that the vertical spiral inductors can achieve better performance and smaller footprint than the in-plane ones.

I. INTRODUCTION

High-performance on-chip inductors are critical for enabling integrated wireless communication systems. Planar spiral inductors that lie in the substrate plane are widely used in radio frequency integrated circuits (RFICs). However, such in-plane inductors involve substrate loss and parasitics (especially on silicon substrate) [1-2]. As a result, their quality factor and self-resonance frequency are generally low. Oftentimes, discrete inductors with better performances have to be used to meet the system performance requirement. However, the use of discrete components introduces parasitics (associated with wire leads), making the system integration and miniaturization more difficult. Also, conventional spiral inductors usually have relatively large footprints, which decreases the potential density of integration and is especially undesirable when the inductors are made on costly III-V compound semiconductor substrates.

Direct, monolithic integration of high performance inductors with integrated circuit elements provides several advantages. First, smaller parasitics can be achieved due to shorter interconnects. Second, it could potentially make wireless communication devices more compact and reliable. Third, it would reduce the fabrication costs of RF microsystems by eliminating assembly steps encountered in the multi-chip module approach.

In recent years, much effort has been made to improve the performance of on-chip spiral inductors. A common theme of research is aimed at increasing the quality factor by reducing losses associated with substrate leakage and decreasing the coil resistance. Certainly, the performance can be improved by using low-loss materials and substrates such as gallium arsenide [3-5]. However, silicon substrates are of low costs and therefore prove to be attractive to commercial RFIC development. Published research work for improving the performance of inductors on silicon substrates generally fall into two major categories: (1) applying micromachining technologies to separate the inductors from the substrates [6-13]; (2) using post-fabrication assembly processes to tilt the inductor away from the substrate surface [14-15].

It is important to note that an optimal inductor solution would need to provide not only good performance but also compatibility with the industrial-standard foundry process. In this regard, micromachining steps such as bulk etching and the use of thick sacrificial layers tend to introduce issues of compatibility with existing foundry processes. Also, the large footprints issue of the inductor is still not solved.

In our opinion, the second approach is more promising, which could result in both improved performance and reduced footprints. We believe that such a process is more likely to be

accepted by the IC foundry because the process can be appended to existing process flow and the inductor can be added to existing IC chips as superstructures.

II. DESIGN CONCEPT

1. PDMA Process

Inductors with spiral coils that are lifted out of the substrate plane have been reported [14-15]. The assembly process proposed in [14] is reported to work with thin metal structures. This may limit its use in assembling spiral inductors with thick metal films (e.g., several micrometers of thickness) for the purpose of reducing series resistance. The assembly process reported in [15] relies on the phase change of manually placed solder spheres. This process requires individual deployment of small solder spheres on the substrate and thus is not suitable for mass production.

We have developed a new 3-D microstructure assembly process called plastic deformation magnetic assembly (PDMA). Using the PDMA process, surface micromachined structures can be bent out of substrate plane permanently and maintain their profile without outside energy or force input. In our opinion, this technique offers two important advantages. First, the process is simple and involves only three layers of thin films (two structural layers and one sacrificial layer). Secondly, the fabrication process is efficient and can be conducted in parallel at wafer scale.

The development of the PDMA process has been discussed in [16]. Since this paper focuses on discussing applications enabled by the PDMA process, it is necessary to briefly describe its basic concept (Fig. 1). For simplicity, we use a surface micromachined cantilever as an example. First, a surface-micromachined cantilever is fabricated on top of a substrate, with one end directly anchored to the substrate and the remaining portion lying on a sacrificial spacer. The cantilever is made of ductile metals such as gold, aluminum or copper. These materials have relatively low yielding strength and hence can be plastically bent more easily compared with other metal materials. Since the cantilever is made of metal, electrical leads between the lifted structure and the substrate surface can be easily established.

A piece of magnetic material is then attached to the cantilever. For example, a ferromagnetic material, Permalloy ($Ni_{80}Fe_{20}$) can be electroplated onto the cantilever. Areas of the cantilever that is covered by the magnetic material is generally much stiffer compared to areas that are not covered. Specifically, a segment of the cantilever between the anchor and one end of the magnetic piece (closest to the anchor) is thin and can bend under an applied moment.

Next, the cantilever is "released" from the substrate by removing the sacrificial layer (Fig. 1a). If an external magnetic field (with a field intensity denoted as H_{ext}) is applied from underneath the substrate, the magnetic piece on the cantilever will be magnetized in the applied magnetic field. As a result, the torque generated in the magnetic material piece will bend the cantilever off the substrate (Fig. 1b). The bending angle of the cantilever θ increases with the magnitude of H_{ext}. When the bending angle reaches a certain threshold, the bending region will encounter irreversible plastic deformation as the internal stress exceeds the yield strength of the cantilever material. After the magnetic field is removed, the cantilever will remain at a certain rest angle ϕ off the substrate (Fig. 1c). The angle ϕ may be smaller than the maximum value of θ. However, the difference may be quite small. Details of the mechanical modeling and design rules for the PDMA process can be found in [16].

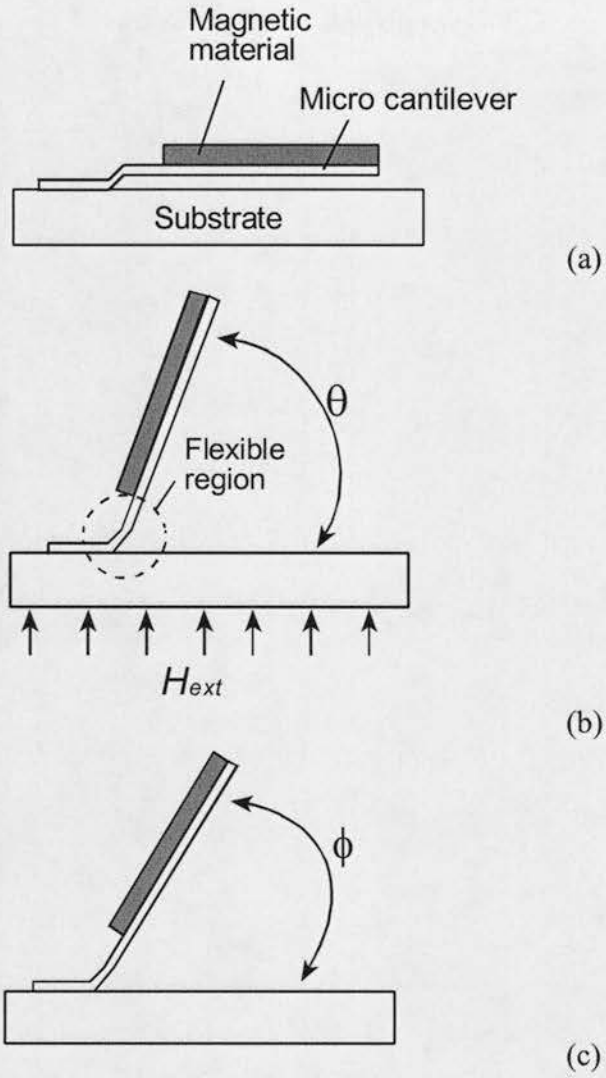


Figure 1 Schematic diagram of the PDMA process.

2. Vertical spiral inductors

Fig. 2 illustrates the general concept of developing on-chip vertical spiral inductors using the PDMA process. The starting substrate may contain integrated circuit elements such as resistors, diodes or transistors (Fig. 2a). An in-plane spiral inductor is then fabricated on the substrate (Fig. 2b). The spiral inductor consists of two metal layers and one dielectric layer. The first metal layer forms the coil. The second metal layer connects the inner end of the spiral coil to an anchor outside the periphery of the coil to complete the coil continuity. A dielectric layer prevents the second-layer metal from contacting the first-layer metal. The spiral coil lies on top of a patch of sacrificial material. Magnetic materials can be placed on top of the planar coil by overlapping with the coil patterns made in the first metal layer. It may be possible to have the in-plane inductor to overlap with circuit elements to maximize the efficiency of chip space.

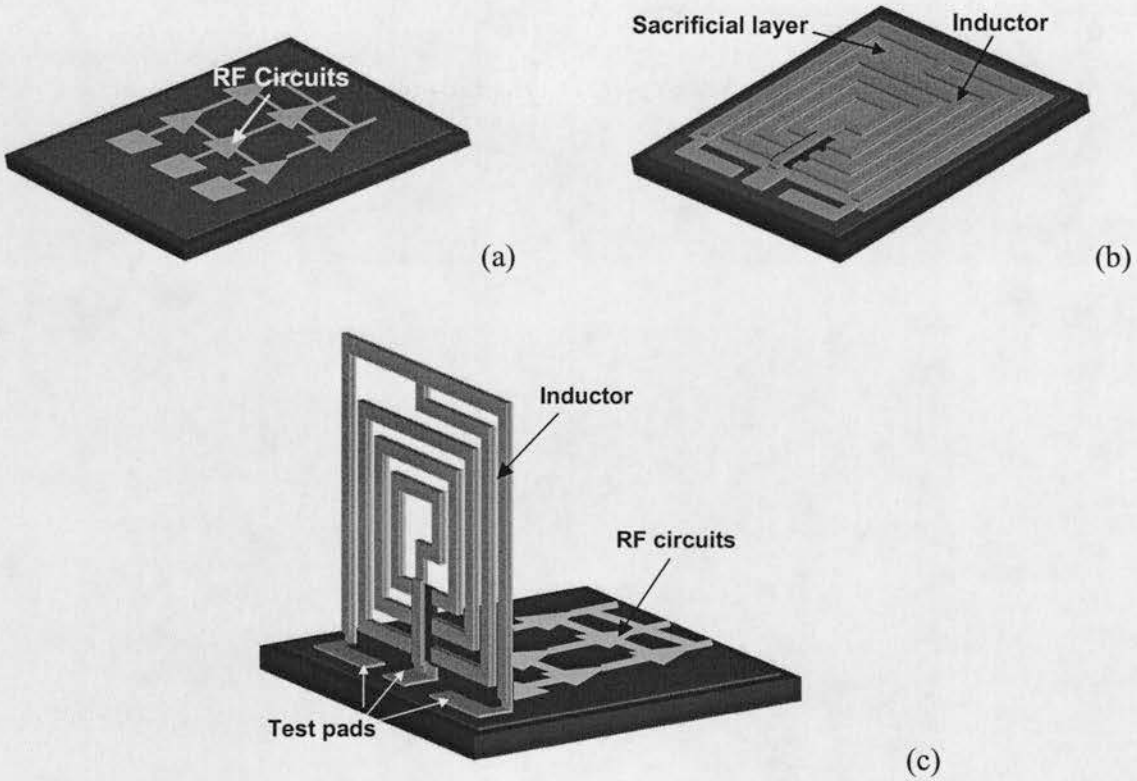


Figure 2 Schematic diagram of building a vertical spiral inductor using the PDMA process.

After the sacrificial layer is removed to free the planar coil, the spiral inductors are assembled to their vertical position using the PDMA process (Fig. 2c). The vertical planar spiral inductors are designed as a one-port co-planar waveguide (CPW) configuration with three test pads to facilitate testing with Cascade® on-wafer probes and network analyzers.

Since the vertical spiral inductors are raised away from the substrate, the substrate loss, parasitics, and also the footprints of the inductors are reduced. The coupling between vertical inductors and the substrate is generally much less than that of the in-plane ones. Thus, the vertical inductors can be initially patterned over circuit elements, essentially increasing the potential density of integration. Moreover, this PDMA-based process provides unique advantages over the aforementioned lifting processes. Spiral inductors with either thin or thick metallization can be assembled. The rotation angle of the inductor can be adjusted during the assembly. No additional supporting structures are needed to hold the vertical inductors after the assembly.

3. On-chip solenoid inductors

Besides spiral inductors, solenoid inductors can also be useful in RFICs. Several research work on on-chip solenoid inductors have been reported [17-19]. In [17], an alumina core is manually placed onto the substrate and copper windings are directly deposited around the core using a mould formed by 3-D laser photolithography. In [18] and [19], multiple layers of electroplated metals are used to make the 3-D solenoid structures. The cross-section area of the on-chip solenoid inductor depends on the height of the electroplated posts.

In this paper, we present an alternative method to form on-chip solenoid inductors with nearly arbitrary cross-section shapes and dimensions (Fig. 3). Different from the processes discussed above, the 3-D winding structures are not made by direct 3-D construction, but by the assembly of 2-D (two dimensional) multi-layer structures. First, a metal layer (Metal 1) is deposited onto the substrate and patterned (Fig. 3a). Multiple parallel metal traces are formed. Second, a second metal layer (Metal 2) is deposited and patterned to form curved wire leads (Fig. 3b). The two metal layers are separated by a sacrificial layer between and connected only at via holes, which are located at the ends of the parallel lines in Metal 1. Magnetic material is then electroplated to overlap with Metal 2 patterns. Next, the sacrificial layer is removed and the PDMA process is used to assemble the top-level winding structures (Metal 2) into vertical position to form a 3-D solenoid inductor (Fig. 3c).

This method allows two unique capabilities. First, solenoid with arbitrary cross-section can be realized. Secondly, relatively large volume of solenoid can be fabricated by incorporating metal thin films. Magnetic cores are currently not integrated with the prototype solenoid inductors.

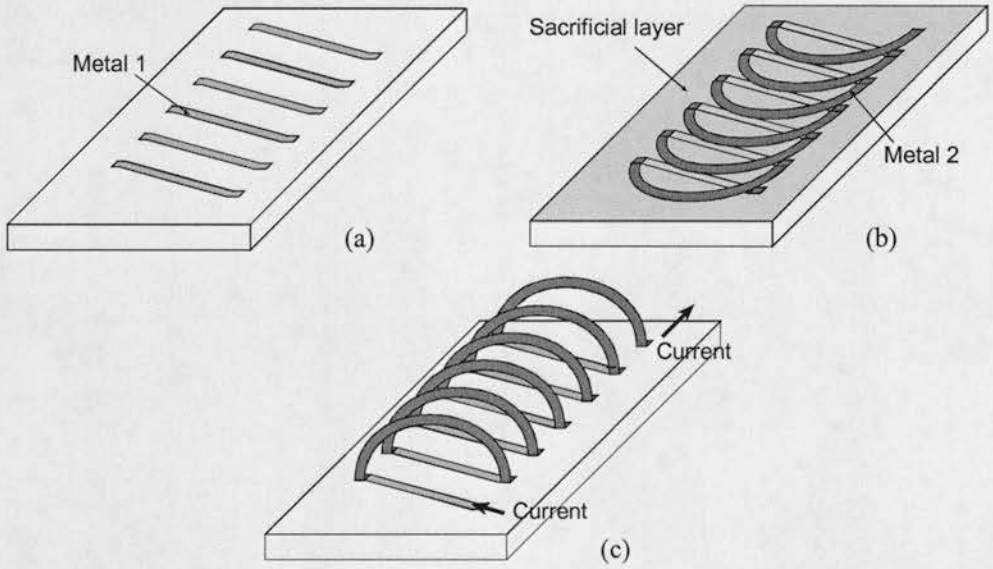


Figure 3 Schematic diagram illustrating the concept of on-chip solenoid inductor development using the PDMA process.

III. Development of On-chip Vertical Spiral Inductors

So far, the development of on-chip vertical spiral inductors consists of two phases. In the first phase, we aimed to demonstrate the proof-of-concept prototype. Some results have been previously reported in [16] and [20]. In the second phase, we improved the design and the fabrication process to achieve higher quality factor.

1. First-generation on-chip vertical spiral inductors

The fabrication process of the first-generation on-chip vertical spiral inductors is shown in Fig. 4. The inductors are fabricated on a silicon substrate coated with a 0.6-μm-thick silicon

nitride layer serving as dielectric insulation. However, this process also allows inductors fabrication directly on glass or polymer substrates.

First, a 0.5-μm-thick silicon oxide layer is deposited and patterned to serve as the sacrificial layer (Fig. 4a). A 0.5-μm-thick gold layer is deposited onto the substrate and patterned to make the spiral coil of the inductor (Fig. 4b). Part of the coil conductor overlaps with the sacrificial layer while the remainder of the coil conductor deposited directly on the substrate, forming a solid anchor. Subsequently, a 2.5μm-thick CYTOP® film (CYTOP-809M from Asahi Glass Corporation) is spun onto the gold layer and patterned as the dielectric spacer (Fig. 4c). A 1.5-μm-thick copper layer is deposited and patterned to make the top conductor used to complete the spiral coil (Fig. 4d). A 5-μm-thick Permalloy layer is electroplated onto the copper and gold surfaces. The Permalloy film increases the stiffness of the coil (Fig. 4e). After the oxide sacrificial layer is etched and the inductor structure is released from the substrate (Fig. 4f), the entire inductor structure is assembled into vertical position using the PDMA process (Fig. 4g). Fig 5 shows a first-generation, 4.5 nH vertical spiral inductor fabricated using the process discussed above.

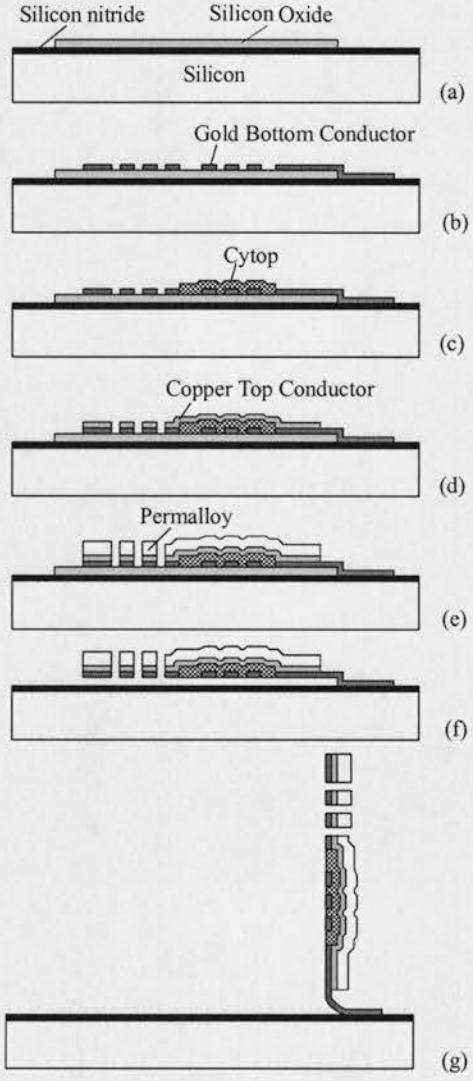
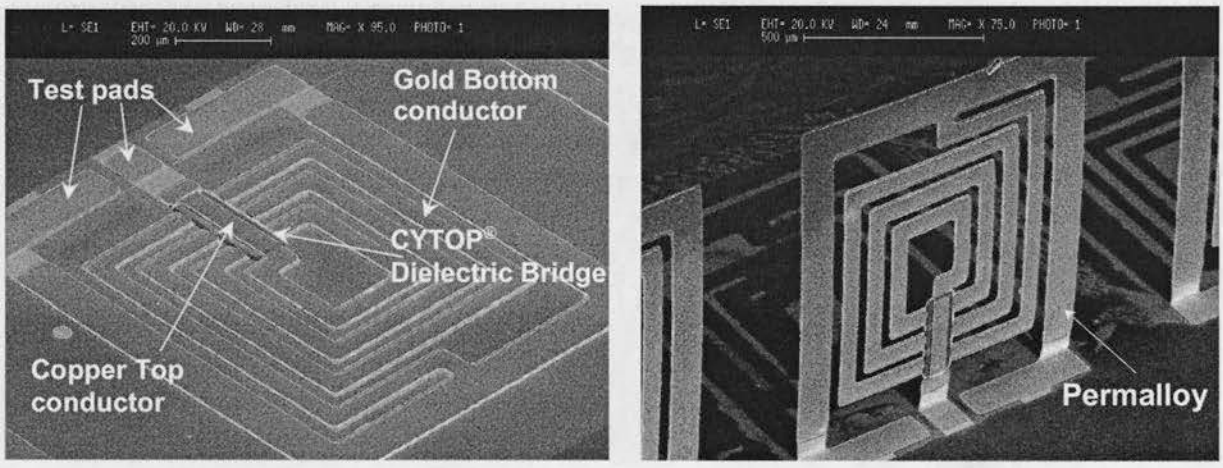


Figure 4 Schematic diagram of the fabrication process of the first-generation on-chip vertical spiral inductor.

The S_{11} parameter of the inductors is measured from 50 MHz to 4 GHz using an HP 8510C network analyzer and a Cascade® coplanar GSG-150 probe. The One-port Short-Open-Load calibration technique is used. The performance of the inductor is also estimated using a comprehensive simulation tool (ADS by Agilent). Fig. 6 shows the simulated and measured S_{11} parameter results of the spiral inductor shown in Fig. 5 before and after the PDMA assembly. The effects of the probing pads that feed the inductors are de-embedded. The extracted quality factor Q as a function of frequency is shown in Fig. 7. The Q factor is estimated by using the following procedure. First, we experimentally measure the S_{11} parameter of the spiral inductor (including the feeding pads) and that of a test structure with only the feeding pads. Second, the one-port impedance of the inductor is calculated from the de-embedded S_{11} parameter. The Q factor is estimated by dividing the imaginary part of the impedance (reactance) with the real part of the impedance (resistance). When the spiral inductor is lying within the substrate plane, it has a peak quality factor of 3.5 and its self-resonance frequency is about 1 GHz. After the PDMA assembly, the same inductor exhibits a peak quality factor of 12 and a self-resonance frequency of well above 4 GHz.



(a) (b)

Figure 5 Scanning electron micrographs of a 4.5 nH first-generation on-chip spiral inductor: (a) the spiral inductor lies in the substrate plane before the PDMA assembly, (b) the inductor stands above the substrate after the PDMA assembly.

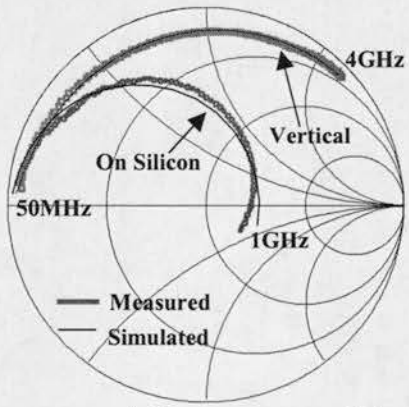


Figure 6 The simulated vs. measured S_{11} parameter of the spiral inductor before and after the PDMA assembly.

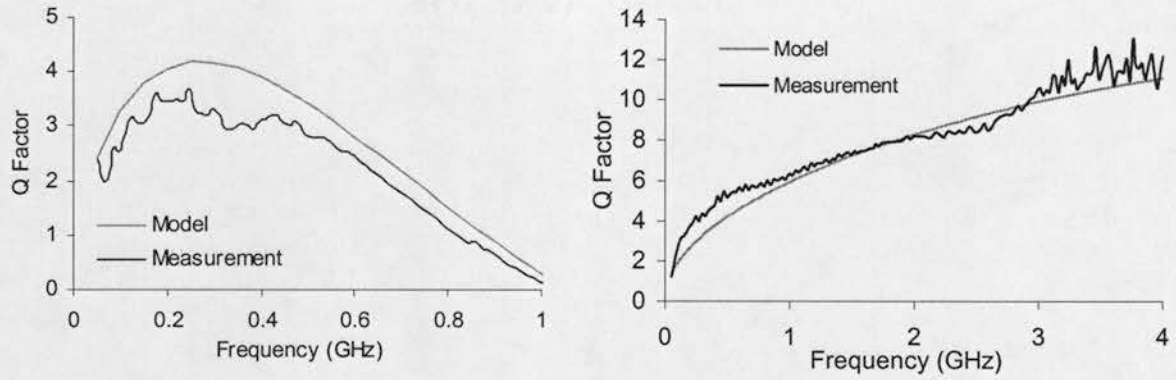


Figure 7 The quality factor Q of the spiral inductor extracted from the simulated and measured S_{11} parameters: (a) before the PDMA assembly, (b) after the PDMA assembly.

2. Second-generation on-chip vertical spiral inductors

In the development of the second-generation on-chip vertical spiral inductors, several modifications were made in the first-phase process to improve the inductor's quality factor.

First, in order to reduce the series resistance of the inductor, the spiral coil of the second-generation inductor is made of 10-μm-thick copper layer instead of the 1.5-μm-thick layer used in the first generation. An electroplating process is used to realize thick copper layers due to its much higher deposition rate than evaporation.

Second, the magnetic piece used in the PDMA process is removed from the inductor after the PDMA assembly. It is found out that the presence of Permalloy makes the position of the assembled inductor susceptible to external magnetic disturbance. Moreover, Permalloy is believed to increase the series resistance of the spiral coil and degrade the inductor's quality factor, due to its relatively low conductivity and high permeability [21,22]. The high permeability of Permalloy decreases the skin depth, which results in higher effective series resistance at the frequencies where the inductor may operate.

Third, in order to reduce current crowding in the spiral coil, we used circular spirals instead of rectangular ones, and increased the open space at the center of the spiral coil [23-25].

A schematic illustration of the fabrication process of the second-generation on-chip vertical spiral inductors is shown in Fig. 8. First, a 0.2-μm-thick aluminum film is deposited onto a substrate and patterned to serve as the first sacrificial layer (Fig. 8a). A 0.3-μm-thick copper layer is deposited, which is followed by the electroplating of 10-μm-thick copper layer (Fig. 8b). Second, a 10-μm-thick photoresist (AZ 4620) film is spun onto the substrate and baked to realize the dielectric spacer (Fig. 8c). Third, a 0.3-μm-thick copper layer is deposited, which is followed by the electroplating of a 10-μm-thick copper thin film (Fig. 8d). Next, the second sacrificial layer, a 10-μm-thick photoresist film (AZ 4620), is spun onto the substrate and baked to completely cover the electroplated copper coil structure. Finally, a 0.3-μm-thick copper layer is deposited to serve as the seed layer of a subsequent electroplating of a 20-μm-thick layer of Permalloy (Fig. 8e).

After the fabrication, the first sacrificial layer is removed (Fig. 8f) and the PDMA assembly is performed (Fig. 8g). Then, the second sacrificial layer is completely removed, allowing the Permalloy piece to be detached from the copper inductor structure (Fig. 8h).

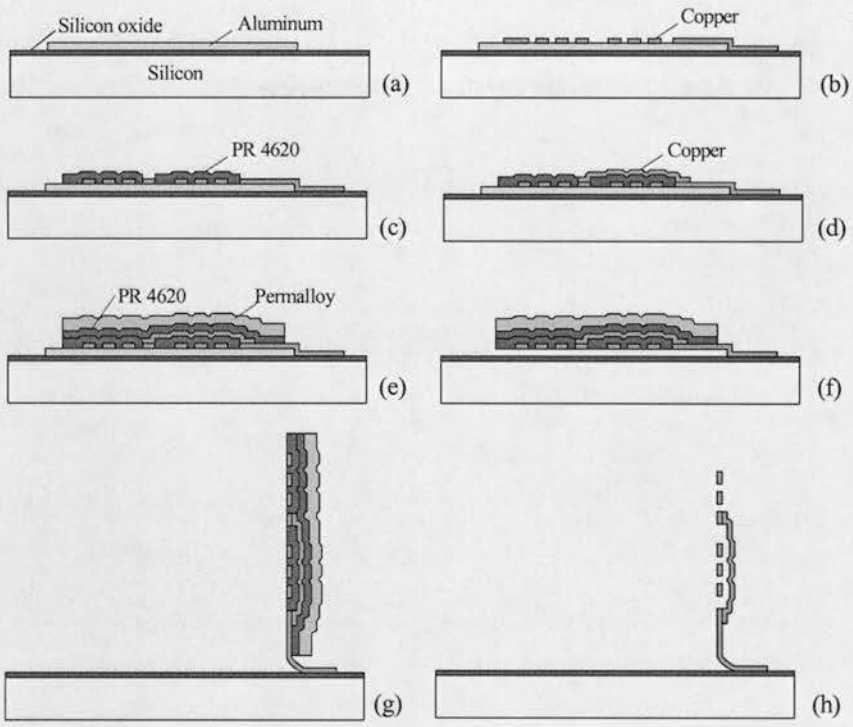


Figure 8 Schematic diagram of the fabrication process of the second-generation vertical spiral inductor.

Scanning electron micrographs of an on-chip spiral inductor (with nominal inductance of 10 nH) fabricated using the above process are shown in Fig. 9. In Fig. 9a, the Permalloy piece is intentionally removed to show the spiral inductor.

The S_{11} parameter of the second-generation vertical spiral inductor is measured from 50 MHz to 10 GHz using an HP 8510C network analyzer and a Cascade® coplanar GSG-150 probe. The measurement is made before and after the assembly for comparison. Fig. 10 shows the measured S_{11} parameter results (without de-embedment) of the spiral inductor shown in Fig. 9a and Fig. 9b. The quality factor Q as a function of operation frequency is extracted from the measured S_{11} parameter results using the same procedure discussed before.

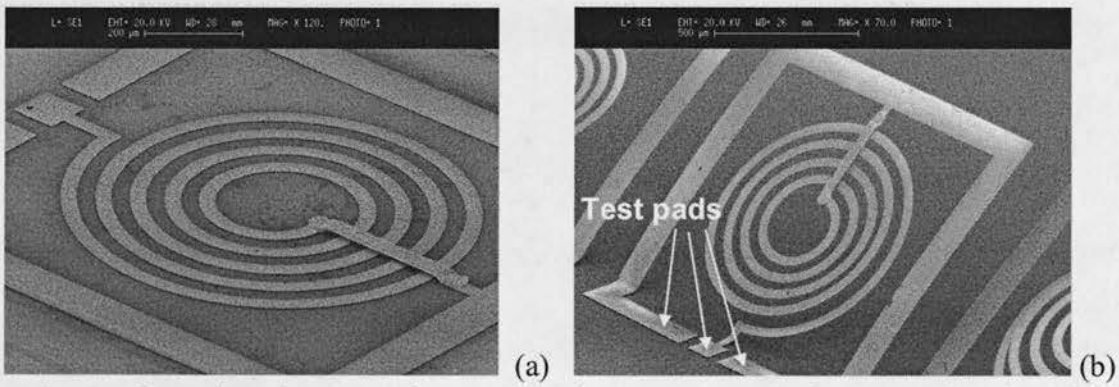


Figure 9 Scanning electron micrographs of a second-generation on-chip spiral inductor: (a) before the PDMA assembly, (b) after the PDMA assembly and removal of the Permalloy piece.

The second-generation inductors produce increased peak quality factor compared with the first-generation ones. When the spiral inductor is on the silicon substrate, it exhibits a peak quality factor of 8 and self-resonance frequency of 1.1 GHz. With the spiral inductor in the vertical position, the peak quality factor and the self-resonance frequency increase to 24 and 5.5 GHz, respectively.

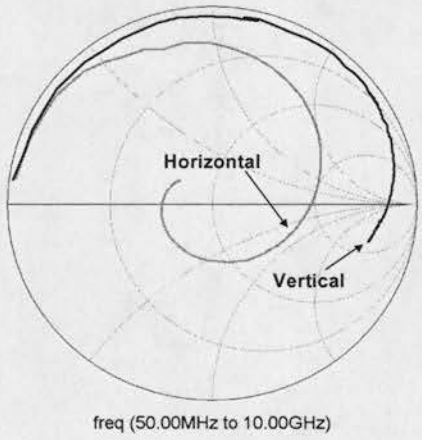


Figure 10 The measured S_{11} parameter (without de-embedment) of the on-chip spiral inductor shown in Figure 9 (a) and (b).

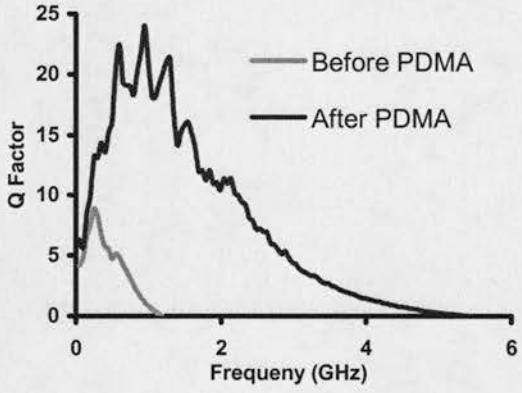


Figure 11 The quality factor Q as a function of frequency extracted from the measured S_{11} parameter results of the spiral inductor shown in Figure 9 (a) and (b).

It is conjectured that higher quality factor and self-resonance frequency can be achieved by further refining the design and fabrication process. However, this is beyond the scope of the current paper, which serves to demonstrate the validity of the methodology.

IV. Development of On-chip Solenoid Inductors

Prototype on-chip solenoid inductors have been successfully fabricated. In our process, gold is used as the material for both metal layers (Metal 1 and Metal 2), while copper serves as the sacrificial layer. This fabrication process can be realized on different substrates, such as semiconductor and glass (Fig.12).

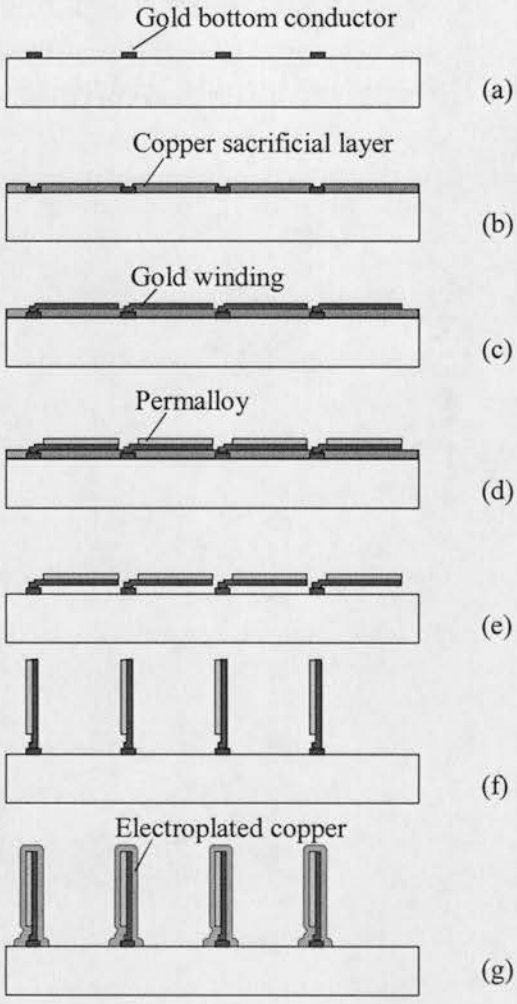


Figure 12 Schematic diagram of the fabrication process of prototype on-chip solenoid inductors.

First, a 0.5-μm-thick gold thin-film is evaporated onto the substrate and patterned to form bottom conductor (Metal 1) traces (Fig. 12a). Second, a 0.3-μm-thick copper is evaporated and patterned to serve as the sacrificial layer (Fig. 12b). Via holes are formed by selectively removing the copper layer to expose the Metal-1 gold layer at the ends of all parallel lines. Third, a second gold layer (0.5 μm thick) is deposited and patterned to define the winding structure (Metal 2), shown in Fig. 12c. The Metal 2 layer contacts the Metal 1 patterns at the via holes. Next, Permalloy material (5 μm thick) is electroplated onto the Metal-2 layer (Fig. 12d). Finally, the copper sacrificial layer (Fig. 12e) is removed and the PDMA process is performed (Fig. 12f). We have demonstrated that it is possible to electroplate copper onto the Metal 1 and Metal 2 winding even after the PDMA assembly to further reduce the series resistance (Fig. 12g).

Scanning electron micrographs of several fabricated prototype on-chip solenoid inductors are shown in Fig. 13. Fig. 13a shows the top view of a solenoid inductor before PDMA is performed whereas Fig. 13b illustrates the same inductor after PDMA assembly. Fig. 13c shows a solenoid inductor with a unique cross-section. Fig. 13d shows a solenoid inductor after copper electroplating.

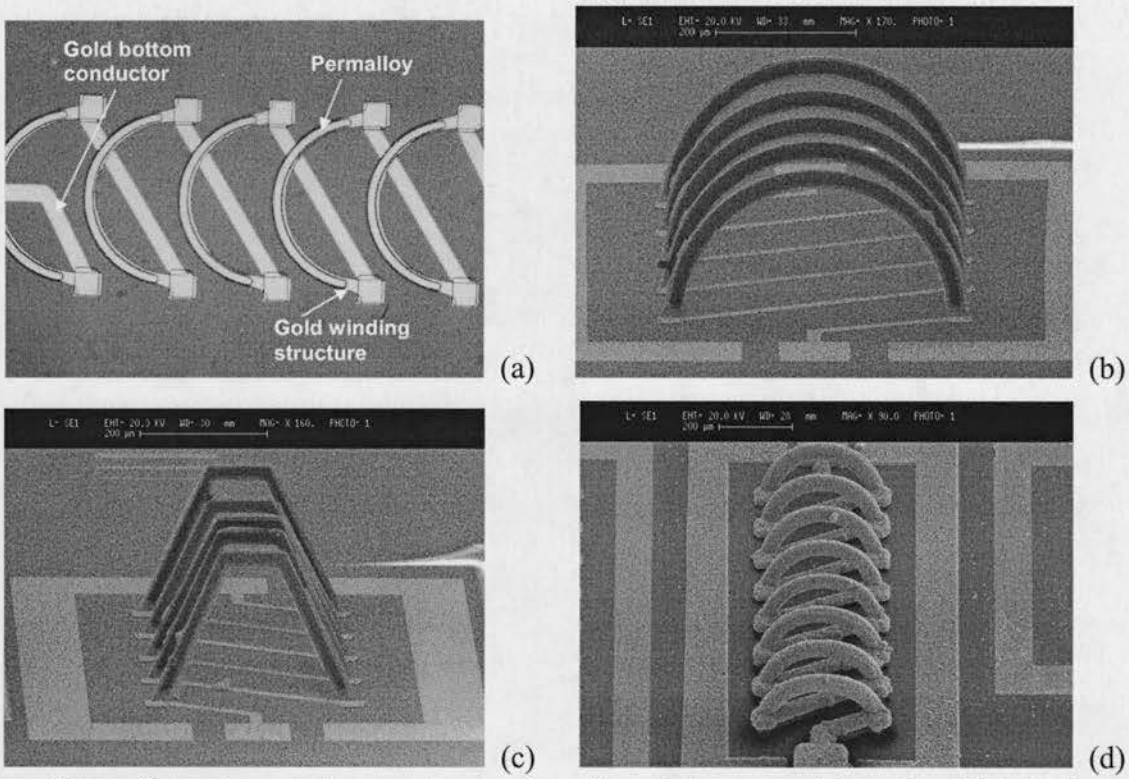


Figure 13 Scanning electron micrographs of prototype on-chip solenoid inductors: (a) before PDMA, (b) and (c) after PDMA, (d) after copper electroplating.

Two-port S-parameter measurement of the fabricated prototype solenoid inductors has been conducted using two Cascade® GSG 150 probes and an HP 8510C network analyzer from 50 MHz to 10 GHz. The measurement results of the solenoid inductor shown in Fig. 13d are shown in Fig. 14. The inductance value and the quality factor Q are extracted from the S-parameter measurement results without deembedding the probe contact pads (Fig. 15). A maximum Q of 10.5 at 1 GHz and an inductance value of 2.5 nH have been achieved. The inductance value can be further increases if the overall length of the inductor is extended.

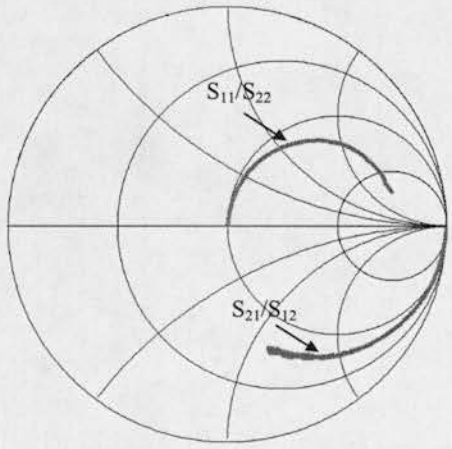


Figure 14 The two-port S-parameter measurement results of the on-chip solenoid inductor shown in Figure 13(d).

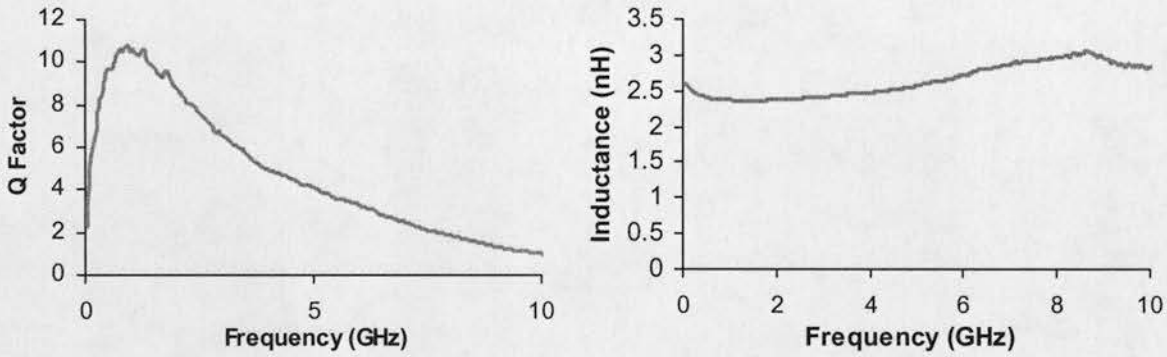


Figure 15 The extracted inductance and the quality factor Q of the on-chip solenoid inductor shown in Figure 13(d).

V. DISCUSSION AND CONCLUSION

Two types of on-chip 3-D inductors have been successfully developed using a novel and efficient three-dimensional assembly process, including vertical spiral inductors and solenoid inductors. The vertical spiral inductors are first fabricated on the substrate and then assembled into vertical position. Experimental results show that they exhibit higher quality factor and resonant frequency than their in-plane counterparts due to reduced substrate loss and parasitics. For the solenoid inductors, 2-D winding structures are first fabricated on the substrate and then assembled into vertical position to form a complete solenoid structure. On-chip solenoid inductors with different winding shapes and cross-section areas have been demonstrated for the first time. The fabrication processes proposed for both vertical spiral inductors and solenoid inductors are compatible with different substrates and current RFIC fabrication foundry.

Though the PDMA-based 3D inductors are presented in the context of RF circuit design, other applications exist or will be enabled by the proposed techniques, such as active control of power management devices within an integrated circuit. Integrated power electronic (dc-dc) converters have smaller size, higher reliability, faster dynamic response, and better energy efficiency [26]. However, the major limitation of integrated power converters has been the passive components, which occupy up to 90% of the total space of the converter and are very lossy at the high switching frequencies they operate [27]. If the PDMA-enabled 3D inductors are applied, the power and space efficiency improvements will be substantial. The authors are currently pursuing a prototype of this concept.

VI. ACKNOWLDGMENT

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Development of Vertical Planar Coil Inductors Using Plastic Deformation Magnetic Assembly (PDMA)

Jun Zou, Josh G. Nickel, Drew Trainor, Chang Liu, and Jose E. Schutt-Aine
Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign
1406 W. Green St., Urbana, IL 61801
Urbana, IL 61801, USA
Email: junzou@uiuc.edu

Abstract—**This paper presents the results of the development of a vertical planar coil inductor. The planar coil inductor is first fabricated on silicon substrate and then assembled to the vertical position by using a novel 3-Dimensional bath-scale self-assembly process (Plastic Deformation Magnetic Assembly (PDMA)). Inductors of different dimensions are fabricated and tested. The S-parameters of the inductors before and after PDMA are measured and compared, demonstrating superior performance due to reduced substrate effects and also increased substrate space savings for the vertical planar coil inductors.**

I. Introduction

With the development of integrated wireless communication systems, on-chip inductors with satisfactory performance (enough quality factor and self-resonant frequency) are required. However, the conventional planar coil inductor suffers from substrate losses and parasitics since it is directly fabricated onto conductive substrate over a very thin dielectric layer [1].

In recent years, much effort has been made to improve the performance of planar coil inductors. Metal materials with higher conductivity or thicker metal layers are utilized to decrease the resistance of the coil. Meanwhile, different methods are proposed to reduce the substrate loss and parasitics, including removing the substrate underneath the inductor [2], applying a thick polymide layer to separate the inductor farther away from the substrate [3], etc.

More recently, planar coil inductors levitated above the substrate are realized using a sacrificial metallic mode (SMM) processes [4]. 3-Dimensional solenoid on-chip inductors developed by using 3-D laser lithography or surface micromachining technology have also been demonstrated [5,6].

This paper reports vertical planar coil inductors developed by using a novel 3-D self-assembly process-Plastic Deformation Magnetic Assembly (PDMA). Experimental results show that the vertical planar coil inductor suffers less substrate loss and parasitics than the conventional horizontal counterparts, and thus can achieve a higher quality (Q) factor and self-resonant frequency. Another major advantage of the vertical inductors is that they have almost zero footprints and thus occupy much smaller substrate space.

II. Plastic Deformation Magnetic Assembly (PDMA)

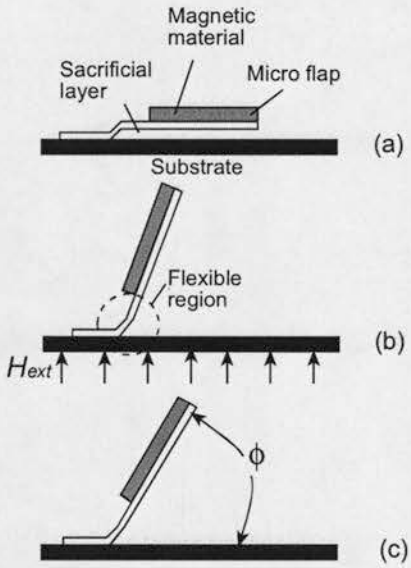


Fig. 1 A schematic illustration of a Plastic Deformation Magnetic Assembly process (PDMA)

PDMA is the key technology to realize the vertical planar coil inductors. A detailed discussion of this assembly process will be presented in other publications. A brief introduction of PDMA is given below by using a cantilever beam as an example. Note that the region near the fixed end is intentionally made more flexible. First, a cantilever beam with a piece of magnetic material attached

to its top surface is released from the substrate by etching away the sacrificial layer underneath (Fig. 1(a)). Next, a magnetic field H_{ext} is applied, the magnetic material piece is magnetized and the cantilever beam will be rotated off the substrate by the magnetic torque generated in the magnetic material piece (Fig. 1(b)). If the structure is designed properly, this bending will create a plastic deformation in the flexible region. The cantilever beam will then be able to remain at a certain rest angle (ϕ) above the substrate even after H_{ext} is removed (Figure 1(c)). By using ductile metal (e.g. gold) in the flexible region, a good electrical connection between the assembled structure and the substrate can be easily achieved, which is suitable for RF applications.

After the vertical assembly, the structures can be further strengthened and the magnetic material can be removed if necessary. If the magnetic field is applied globally, then all the structures on one substrate can be assembled in parallel.

III. Design and Fabrication of Vertical Planar Coil Inductors

The core structure of the vertical planar coil inductor is identical to the conventional horizontal one, which consists of two metal layers and one dielectric layer between. As a general rule, high conductivity metal and low loss dielectric material should be used. In addition to this requirement, the structure of the inductor should facilitate the implementation of PDMA.

The vertical planar coil inductor utilizes one-port co-planar waveguide (CPW) configuration with 3 test pads (Ground-Signal-Ground) with a pitch of 150μm. The three test pads also serve as the anchor of the vertical inductors on the substrate.

3.1 Material consideration

Gold is used as the material for the bottom conductor (the coil). Gold is a ductile material with high conductivity. It is an ideal plastic deformation material for the implementation of PDMA. Copper is selected as the material of the top conductor (the bridge). Copper is also a high conductivity metal and its processing is compatible with the gold bottom conductor during the fabrication.

Silicon oxide and nitride are good dielectric materials available in silicon IC process. However, they are not suitable for vertical planar coil inductors due to high internal stress and poor adhesion on metal surface.

CYTOP® amorphous flurocarbon polymer is selected as the dielectric spacer of the vertical inductors. The electrical properties of CYTOP® film are similar to those of Polyimide and Telfon®. However, it has a better adhesion on metal surfaces and chemical stability.

In order to implement PDMA, Permalloy (NiFe) is electroplated onto the surface of the gold and copper structures. The Permalloy layer will provide the magnetic force necessary for PDMA and enough stiffness to the inductor structure in the vertical position.

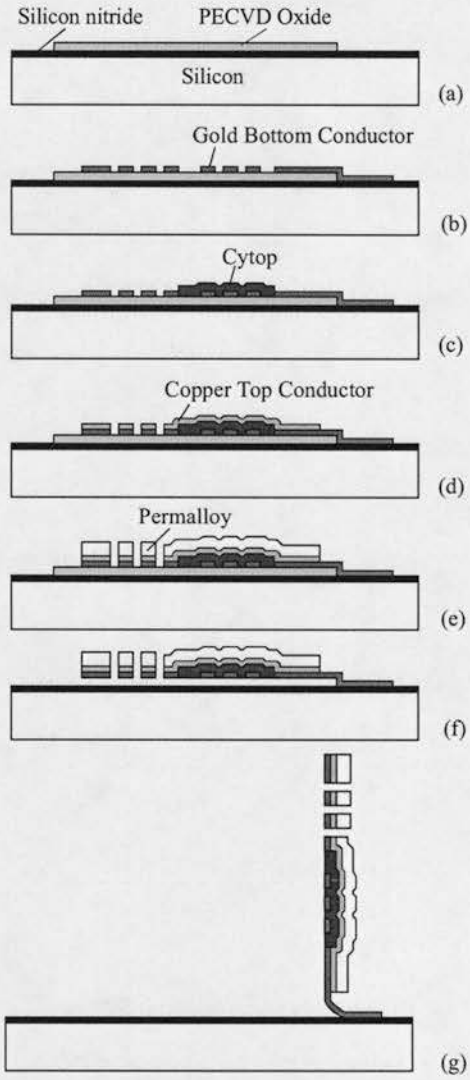


Fig. 2 A schematic illustration of the fabrication and PDMA assembly of vertical planar coil inductors.

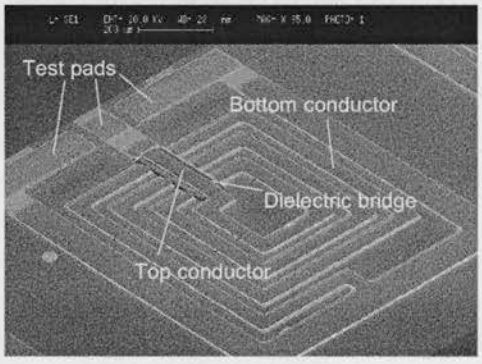
3.2 Fabrication process

A brief illustration of the entire fabrication and assembly process is shown in Fig. 2. The substrate is a silicon wafer with a 0.6μm-thick nitride layer on top. The fabrication is conducted in the following steps:

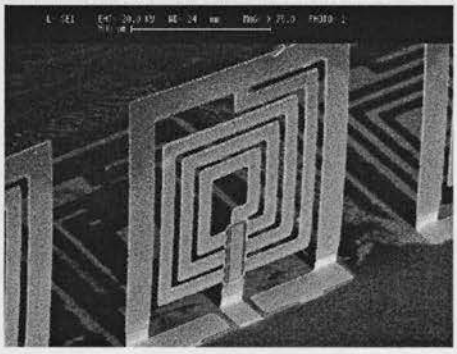
(a) A 0.5μm-thick silicon oxide layer is deposited and patterned to serve as the sacrificial layer for PDMA.

(b) A 0.5μm-thick gold layer is deposited onto the substrate (with sacrificial layer underneath) and patterned to make the bottom conductor (coil) of the inductor.
(c) A 2.5μm-thick CYTOP® film is spun onto the gold layer and patterned to make the dielectric spacer.
(d) A 1.5μm-thick copper layer is deposited and patterned to make the upper conductor (bridge) of the inductor.
(e) A 5μm-thick Permalloy layer is electroplated onto the copper and gold surface.
(f) The oxide sacrificial layer is etched and the inductor structure is released from the substrate.
(g) The entire inductor structure is assembled into vertical position using PDMA.

Scanning electron micrographs of a 4.5nH planar coil inductor before and after PDMA are shown in Fig. 3.



(a)

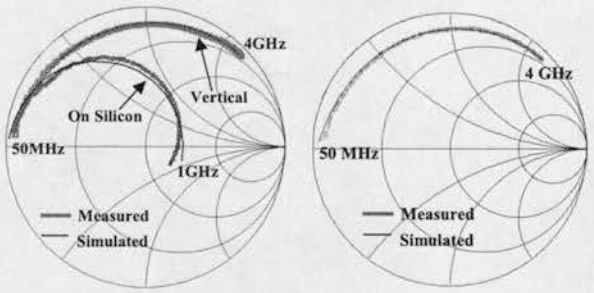


(b)

Fig. 3 (a) A scanning electron micrograph of a planar coil inductor fabricated on the substrate surface before the PDMA assembly; (b) A scanning electron micrograph of the same inductor after the PDMA assembly.

IV. Testing and Measurement Results

The S_{11} parameter of the fabricated vertical planar coil inductors is measured from 50 MHz to 4GHz using an HP® 8510C network analyzer. The S_{11} parameter is first measured while the inductors are on the silicon substrate before PDMA. Next, the inductors are assembled to the vertical position using PDMA and the S_{11} measurement is repeated. The S_{11} parameter of inductors with identical designs fabricated on Pyrex® glass substrate is also measured for comparison.

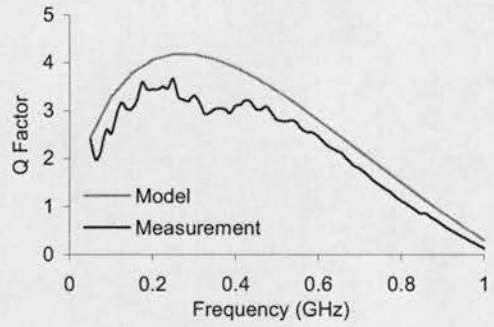


(a) (b)

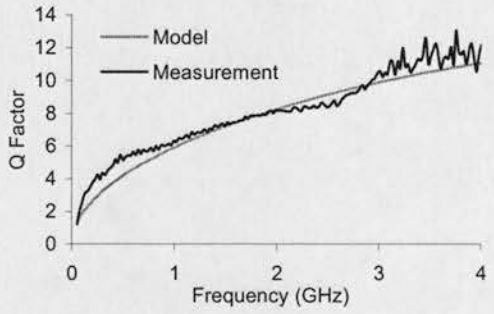
Fig. 4 (a) A Smith chart showing the simulated and measured S_{11} parameter results of the planar coil inductor shown in Fig. 3 before and after PDMA. (b) A Smith chart showing the simulated and measured S_{11} parameter results of an inductor with identical design fabricated on glass substrate. The inductance of both inductors is 4.5nH.

Fig. 4 (a) shows the simulated and measured S_{11} parameter results of the planar coil inductor shown in Fig. 3. The test pads feeding the inductors on which probing occurs are de-embedded. Fig. 4(b) shows the simulated and measured S_{11} parameter results of an inductor with identical design inductor fabricated on Pyrex® glass substrate. The test pads are not de-embedded since the inductor is on glass substrate and the de-embedment has little effect. The simulated data is generated by using a compact circuit model for planar coil inductor presented in [1]. The quality factor (Q) as a function of frequency extracted from both the simulated and measured S_{11} parameter results is plotted in Fig. 5. When the planar coil inductor is on the silicon substrate, it has a peak Q factor of 3.5 and self-resonant frequency of 1GHz. When the inductor is in the vertical position after the PDMA assembly, the peak Q factor increases to 12 and the self-resonant frequency goes well above 4GHz, which are close to those of the inductor on glass substrate.

For the planar coil inductors fabricated on silicon (before assembly), a large insulator capacitance and the substrate resistance dominate at higher frequencies, which leads to a self resonate frequency of about 1GHz. Once the inductors are assembled into the vertical position, the substrate loss and capacitance are effectively removed, which leads to the improvement in the inductor performance. Furthermore, for frequencies far below 1 GHz (where substrate effects are negligible), the glass and silicon inductor measurements correspond exactly, as expected.



(a)



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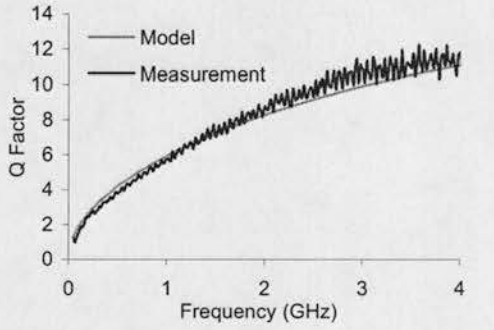

(c)

Fig. 4 The quality factor of the planar coil inductor extracted from the simulated and measured S_{11} parameters: (a) the inductor on silicon before PDMA; (b) the inductor in vertical position after PDMA; (c) an inductor with identical design on glass substrate.

V. Discussion

1) In this work, oxide is used as the sacrificial material for PDMA. Sometimes, oxide is used as the dielectric for IC devices on the same substrate and thus cannot be removed. In this case, the oxide sacrificial layer can be substituted by other materials, e.g. photo resist.
2) In order to facilitate the measurement, the vertical planar coil inductors tested are not strengthened after PDMA. However, the inductor structure can be strengthened after PDMA by using different methods (e.g. Parylene coating) to achieve the necessary stiffness and robustness.
3) While the Q factor of vertical planar coil inductors can be improved by depositing thicker metal layers during the fabrication, experiments are also being conducted to explore various methods to thicken and strengthen the metal layers of the planar coil inductors while they are in the vertical position after the PDMA assembly.

VI. Conclusion

Vertical planar coil inductors have been achieved by using a novel 3-D assembly-Plastic Deformation Magnetic Assembly (PDMA). Vertical planar coil inductors offer two major advantages over conventional on-substrate ones: they occupy much smaller substrate space and suffer less substrate loss and parasitics.

The proposed fabrication and assembly process of the vertical planar coil inductor is compatible with the standard IC fabrication process, and is therefore suitable for various RF ICs.

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Development of a Wide-Tuning-Range Two-Parallel-Plate Tunable Capacitor for Integrated Wireless Communication Systems

Jun Zou, Chang Liu, José E. Schutt-Ainé

Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

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ABSTRACT: This paper reports on the development of a micromachined parallel-plate tunable capacitor with a wide tuning range. Different from conventional two-parallel-plate tunable capacitors, this tunable capacitor consists of one suspended top plate and two fixed bottom plates. One fixed plate and the top plate form a variable capacitor, while the other one provides necessary electrostatic actuation. Among the fabricated prototype devices, a maximum controllable tuning range of 69.8%@1 MHz has been obtained experimentally, exceeding the theoretical limit (50%) of conventional two-parallel-plate tunable capacitors. A component quality factor (Q) of 30@5 GHz and a self-resonant frequency far beyond 5 GHz have been achieved. The fabrication process is compatible with the existing standard IC (integrated circuit) technology, which makes it suitable for integrated wireless communication applications. © 2001 John Wiley & Sons, Inc. Int J RF and Microwave CAE 11: 322–329, 2001.

Keywords: MEMS; tunable capacitor; varactor; wireless communication

I. INTRODUCTION

In future wireless communication systems, integration of low loss passive components is required to increase performance and reduce power consumption and cost. This imposes special challenges on IC (integrated circuit) technology [1–4]. In the past few years, micromachining technology has been applied in the fabrication of integrated wireless communication systems [5] either to improve the performance of existing devices or create novel components. Micromachined RF (radio frequency) components that have been reported so far include inductors [6–8], switches [9–11], phase shifters [12], resonators and oscillators [13–15], and tunable capacitors [16–19], to name a few.

Recently, tunable capacitors based on micromachining technology are under active development. Compared with solid-state varactors, micromachined tunable capacitors have lower loss and potentially greater tuning range. Among all the micromachined tunable capacitors developed to date, the parallel-plate configuration (using electrostatic actuation) is most commonly used. A parallel-plate capacitor can be fabricated using established surface micromachining processes. However, the tuning range of such capacitors is limited to 50% by the *pull-in* effect. The actual achieved tuning range is often much smaller than 50% due to parasitic capacitance (e.g., a measured tuning range of 16% was reported in [16]).

However, various communication applications require a wide tuning range. Different schemes have been adopted to increase the tuning range of the parallel-plate tunable capacitor. Dec *et al.*

Correspondence to: Jun Zou; e-mail: junzou@uiuc.edu.

[17] uses a three-parallel-plate configuration (two suspended plates and one fixed plate on the substrate) to compensate the *pull-in* effect and obtain a tuning range of 87%. The fabrication process for such capacitors requires two layers of structural materials and two layers of sacrificial materials. Yao *et al.* [18] reported a tunable capacitor with a tuning range of 200%. It is based on lateral comb structures (instead of parallel plate) etched by using deep reactive ion etching (DRIE). Feng *et al.* [19] used a thermal actuator in the tunable capacitor to remove the tuning range limit imposed by the *pull-in* effect of electrostatic actuators, and achieved a tuning range of 270%. However, the response of thermal actuators is generally much slower than that of electrostatic actuators.

In this paper, a new electrostatically tunable capacitor design is proposed. This design keeps the simplicity of conventional two-parallel-plate configuration, while overcoming its low tuning range disadvantage. The design concept has been validated by testing the fabricated prototype devices. A maximum controllable tuning range of 69.8% has been obtained experimentally, exceeding the theoretical limit (50%) of conventional two-parallel-plate tunable capacitors. A component quality factor (Q) of 30 at 5 GHz and a self-resonant frequency far beyond 5 GHz are also achieved.

II. THEORY AND DESIGN

A schematic model of conventional two-parallel-plate capacitors is sketched in Figure 1, which consists of one suspended top plate and one fixed bottom plate, with an overlap area of A and initial spacing of x_0 (Fig. 1). When a DC voltage (V_{DC}) is applied across these two plates, the spacing will be decreased to $x_0 - x$. While neglecting the fringe effect, the value of the capacitance (C) and the tuning range can be determined by

$$C = \frac{\varepsilon A}{(x_0 - x)} \tag{1}$$

$$\text{tuning range} = \frac{C - C_0}{C_0} = \frac{x_0 - x}{x_0}. \tag{2}$$

If x is decreased beyond $x_0/3$, the two plates will be snapped into contact by the overwhelming electrostatic force. This phenomenon is called the *pull-in* effect. The value of V_{DC} at $x = x_0/3$ is defined as the *pull-in* voltage (V_{PI}). More detail analysis on the pull-in effect can be found in [20]. The *pull-in* effect limits the maximum controllable tuning range to 50% for an electrostatically actuated two-parallel-plate tunable capacitor [eq. (2)]. In order to achieve a higher tuning range, x has to be tuned beyond $x_0/3$.

The schematic model of the new wide-tuning-range tunable capacitor is shown in Figure 2. It consists of three plates that are designated as E_1, E_2, and E_3. The plate E_1 is a movable top plate suspended by four cantilever beams. The fixed plate E_2 forms a variable capacitor with the plate E_1. The fixed plate E_3 and E_1 are used to provide the electrostatic actuation. A DC voltage (V_{DC}) is applied between plates E_3 and E_1. Thus, the spacing/capacitance between plates E_2 and E_1 can be tuned by adjusting the magnitude of V_{DC}.

The original spacing between plates E_2 and $E_1(d_1)$ is designed to be smaller than the spacing between plates E_3 and $E_1(d_2)$. The values of d_1 and d_2 can be controlled during the fabrication. When the top plate E_1 is pulled down by a distance x at a given applied V_{DC}, the tuning range is derived as

$$\text{tuning range} = \frac{C - C_0}{C_0} = \frac{\varepsilon A/(d_1 - x) - \varepsilon A/d_1}{\varepsilon A/d_1} = \frac{x}{d_1 - x}. \tag{3}$$

This tuning range derivation is valid as long as the *pull-in* effect between plates E_3 and E_1 does not occur when $x < d_2/3$. The discussion of the maximum tuning range falls into two cases. First, if $d_1 > d_2/3$, then the maximum tuning range can be found by plugging in $x = d_2/3$ into eq. (3),

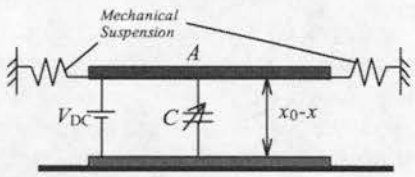

Figure 1. A schematic model of a conventional electrostatically actuated two-parallel-plate tunable capacitor. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

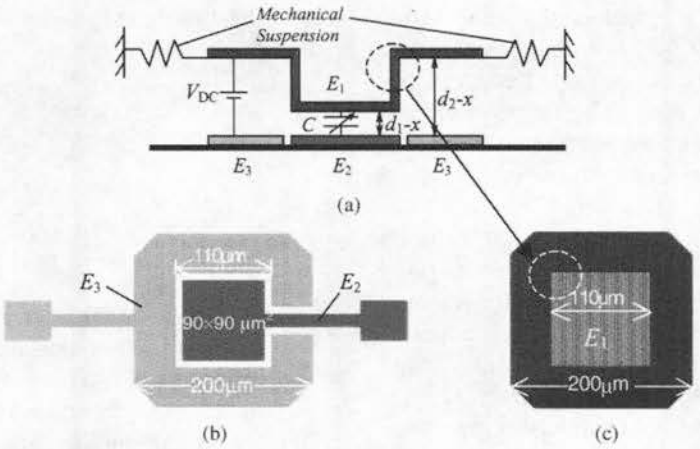

Figure 2. (a) A schematic model of the wide-tuning-range tunable capacitor; (b) a schematic top view of the two fixed plates E_2 and E_3; (c) a schematic top view of the suspended top E_1. The listed geometric parameters are used in the prototype device fabrication. [Color figure can be viewed in the online issue, which is available at www.interscience.com.]

thus

$$\text{maximum tuning range} = \frac{d_2}{3d_1 - d_2}. \quad (4)$$

Secondly, if $d_1 \leq d_2/3$, the maximum travel distance of plate E_1 will be equal to d_1. In other words, the *pull-in* effect will not occur. Assuming the plates E_1 and E_2 can be pulled in to infinitely close distance ($x = d_1 - \varepsilon$), the maximum tuning range is

$$\text{maximum tuning range} = \frac{d_1 - \varepsilon}{\varepsilon} \Rightarrow \infty. \quad (5)$$

Theoretically, an arbitrary tuning range can be achieved controllably. In reality, the achievable tuning range value also depends on other factors, such as surface roughness and curvature of E_2 and E_1.

III. FABRICATION

A surface micromachining process is used to fabricate the prototype devices with a Pyrex® glass wafer (1 mm thick) as the substrate. A unique process to realize the variable-height sacrificial layer [corresponding to $d_1 = 2$ μm and $d_2 = 3$ μm in Fig. 2(a)] is developed. Thermally evaporated gold thin film is used as the material of the two fixed bottom plates E_2 and E_3, whereas the suspended top plate E_1 is made of electroplated Permalloy (nickel–iron alloy). Permalloy can be deposited by electroplating up to 200 μm with good surface smoothness and relatively low stress [21].

Copper is used as the sacrificial layer material. Copper can be deposited using thermal evaporation and etched by one copper etchant ($HAC:H_2O_2:H_2O$ = 1:1:10), which has a very high etching selectivity between copper and the structure materials (Permalloy and gold). The copper layer also serves as the seed layer for Permalloy electroplating.

A brief description of the fabrication process is illustrated in Figure 3. First, a 0.5-μm-thick gold film is thermally evaporated and patterned to form the two fixed plates (E_2 and E_3) and contact pads for the suspended top plate E_1 [Fig. 3(a)]. Secondly, a 1-μm-thick copper film is thermally evaporated and patterned, followed by the thermal evaporation of another 2-μm-thick copper film to make the variable-height sacrificial layer [Fig. 3(b)–(d)]. Thirdly, a 2-μm-thick Permalloy is deposited by electroplating [Fig. 3(e)]. The copper sacrificial layer is then etched and the entire device is released in a supercritical carbon dioxide (CO_2) dryer [Fig. 3(f)] [22]. Scanning electron microscopic graphs of the fabricated prototype devices ae shown in Figure 4. The suspended top plate E_1 is supported by four identical cantilever beams. Four etch holes are intentionally opened to speed up the sacrificial layer etching process.

In the fabricated prototype devices, d_1 and d_2 have the nominal values of 2 and 3 μm, respectively. In this case, d_1 can be tuned to 1 μm before the *pull-in* effect occurs between E_1 and

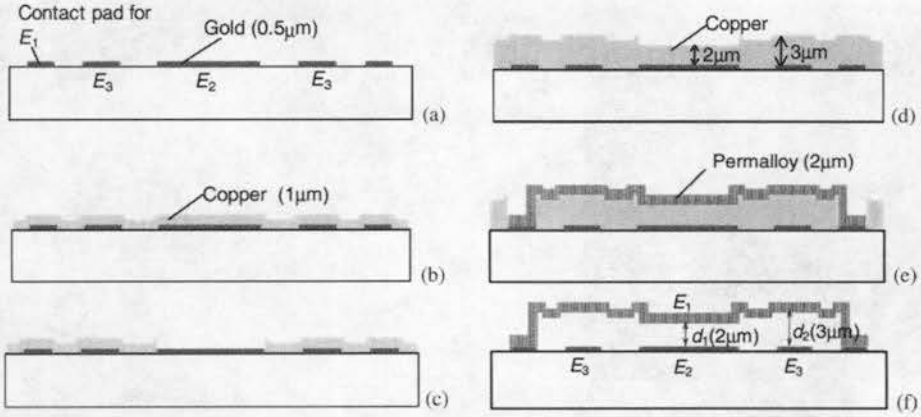

Figure 3. A schematic illustration of the fabrication process for the wide-tuning-range tunable capacitor. [Color figures can be viewed in the online issue, which is available at www.interscience.com.]

E_3, which corresponds to a maximum theoretical tuning range of 100% [eq. (4)] for the variable capacitance between E_1 and E_2.

IV. ELECTROMECHANICAL AND ELECTRICAL ANALYSIS

The static electromechanical characteristic of the wide-tuning-range tunable capacitor design is simulated using the MEMCAD® 4.5 software [23]. The calculated deformation of the suspended top plate at V_{DC} = 18 V is shown in Figure 5, which shows that the suspended top plate (E_1) still remains flat and parallel to E_2 after the deformation. The simulated capacitance–voltage (C–V_{DC}) curve is plotted in Figure 8 together with the measurement data, which shows a maximum tuning range of 90.8%. This value is smaller than the theoretical tuning range of 100% predicted by eq. (4) due to the account of fringe capacitance. The change of spacing d_1 as a function of V_{DC} is plotted in Figure 7 together with the measurement data. When V_{DC} is greater than 19 V, d_1 decreases directly from 1 μm to 0 which means the *pull-in* voltage is about 19 V from this simulation.

The high-frequency behavior of the wide-tuning-range tunable capacitor is simulated using Sonnet *em* Suite® software [24]. The simulated S_{11} parameter at V_{DC} = 0 V is plotted with the measurement data in Figure 9.

V. TESTING AND MEASUREMENT

A. Static Electromechanical Behavior of the Suspension

The surface profile of the tunable capacitor at different values of V_{DC} is measured using the WYKO® NT1000 optical surface profiler. Figure 6(a) and (b) shows the surface profile plotted in

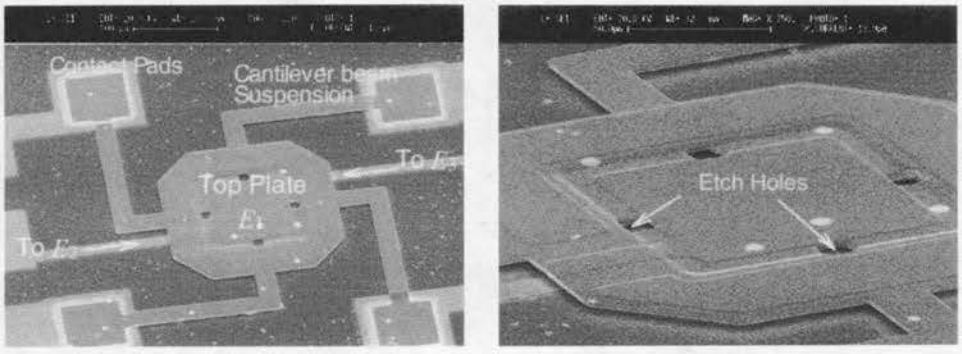

Figure 4. (a)(b) Scanning electron microscopic graphs of the wide-tuning-range tunable capacitor.

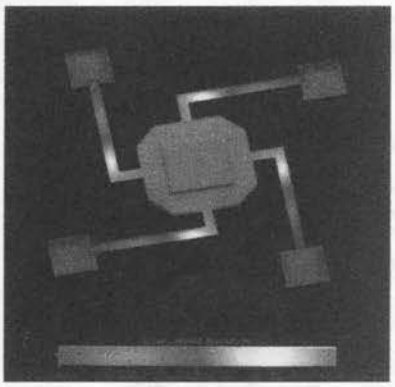

Figure 5. A pseudo-color three-dimensional plot of the deformed suspended top plate (E_1) when V_{DC} = 19 V. The color represents the value of the displacement in z (thickness) direction at each point. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

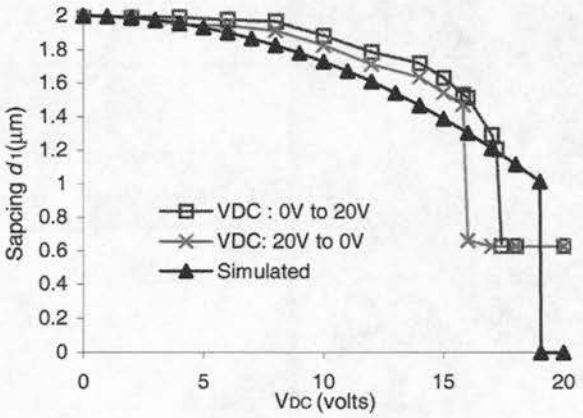

Figure 7. The measured vs. simulated value of the spacing between Plate E_1 and E_3 (d_1) as a function of V_{DC}. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

3D graphs at V_{DC} = 0 V and V_{DC} = 16 V, respectively. In Figure 6(a), the color of the top plate is uniform, which means that the top plate is parallel with the bottom plate at V_{DC} = 0 V. In Figure 6(b), the color of the top plate is not strictly uniform, which means that the top plate has some tilting under the action of electrostatic force due to asymmetry of design of the bottom plate E_3 (Fig. 2).

The value of the spacing (d_1) between the suspended top plate E_1 and the fixed plate E_2 as a function of V_{DC} is extracted from the surface profile measurement (Fig. 7). When V_{DC} increases from 0 to 20 V, d_1 decreases continuously from 2 to 1.2 μm until the *pull-in* effect occurs at V_{DC} = 17.2 V. When V_{DC} decreases from 20 to 0 V, the suspended top plate (E_1) is observed not to recover from the *pull-in* effect until V_{DC} drops to 15.8 V. The possible reason for this hysteresis is stated as follows. When the *pull-in* effect occurs, the suspended top plate and the bottom plate are pulled into close contact. Most likely, surface bonding force will build up. Therefore, the driving voltage has to be reduced to a certain value (e.g., 15.8 V) smaller than the *pull-in* voltage (e.g., 17.2 V), such that the mechanical restoring force of the suspension can overcome the electrostatic force plus the surface bonding force to make the entire top plate recover from the *pull-in* effect.

Another phenomenon observed is that d_1 was decreased to 0.6 μm, instead of zero when the *pull-in* effect occurs. This means that the suspended top plate (E_1) does not fully contact with the fixed plate (E_2). This difference is because the measured spacing is actually obtained by finding the height value at the center of the top

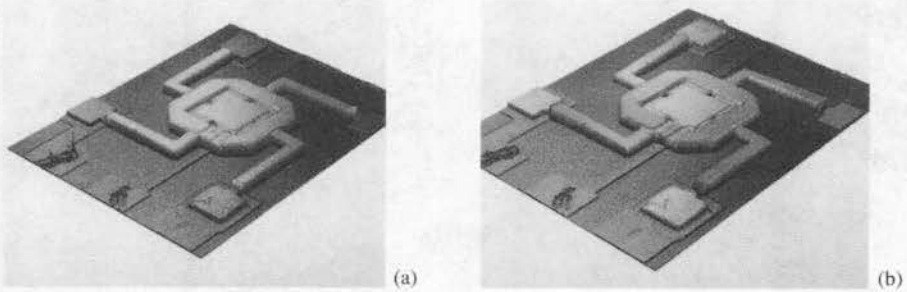

Figure 6. Three-dimensional plots of the measured surface profile of the tunable capacitor by using WYKO® NT1000 optical profiler: (a) V_{DC} = 0 V; (b) V_{DC} = 16 V. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

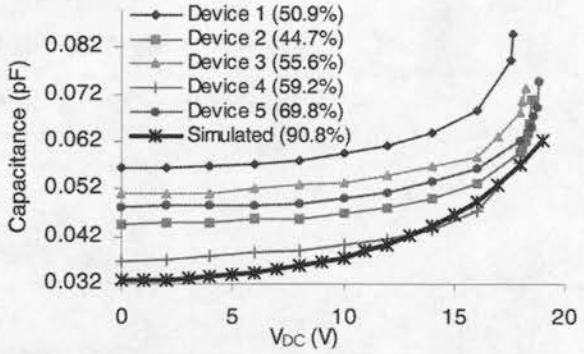

Figure 8. C–V_{DC} measurement of the wide-tuning-range tunable capacitor at 1 MHz using HP4284A precision LCR meter. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]

plate. Due to asymmetry of design and imperfection of fabrication, the top plate could be slightly tilted when it is pulled down by the electrostatic force [Fig. 6(b)]. In this case, the edge of the top plate will touch the bottom plate first when the *pull-in* effect occurs.

B. C–V_{DC} Characterization

Five identical prototype devices fabricated on one substrate are tested using HP 4284A precision LCR meter at the frequency of 1 MHz (Fig. 8). The *pull-in* effect is observed at a DC bias of approximately 17–20 V. The difference in the *pull-in* voltage is found to be introduced by the different stiffness of the four-cantilever beam suspension of each device. The maximum tuning ranges of the five devices are 50.9%, 44.7%, 55.6%, 59.2%, and 69.8%, respectively. The different parasitic capacitance existing in the measurement of each capacitor causes the decrease and variation of the actual achievable tuning range.

C. S_{11} Parameter Measurement

The S_{11} scattering parameter of the wide-tuning-range tunable capacitor (when V_{DC} = 0 V, 5 V, 10 V, and 15 V) is measured using Cascade® co-planar GSG-150 probe and HP 8510B network analyzer from 45 MHz to 5 GHz. The measurement result at V_{DC} = 0 V is plotted in Figure 9, which shows a nearly ideal capacitive behavior in the tested frequency range with a return loss lower than 0.15 dB. The measurement data closely matches the simulation data. The capacitance of the tunable capacitor at different values of V_{DC} bias is extracted from the measured S_{11} data based on a series RC equivalent circuit model (Fig. 10). A component quality factor (Q) of 30 at 5 GHz and self-resonant frequency far beyond 5 GHz have been achieved.

VI. DISCUSSION

For parallel-plate tunable capacitors, the suspension structure and shape of the top plate and bottom plate should be carefully designed to ensure that the suspended top plate will always remain strictly parallel to the bottom plate. Otherwise, the achievable tuning range will be reduced if the suspended top tilts during the operation of the tunable capacitor.

Due to the small but finite intrinsic stress of the Permalloy film, the size of the suspended top plate (E_1) is made smaller than 500 × 500 μm. This limits the base capacitance of the tunable capacitor. One way to achieve a larger capacitance value is to increase the area of the parallel plates. However, this approach requires thin-film

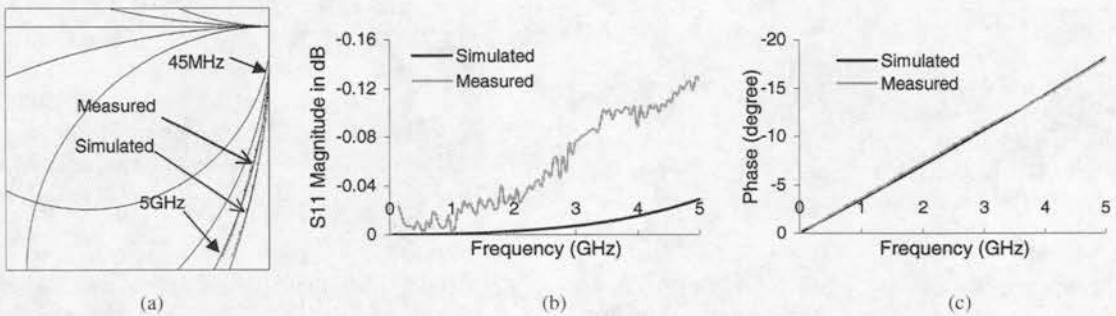

Figure 9. The simulated vs. measured S_{11} parameter of the wide-tuning-range tunable capacitor (45 MHz–5 GHz): (a) Smith chart, (b) magnitude, (c) phase.

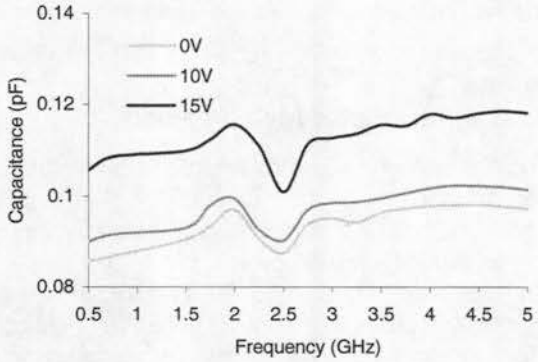

Figure 10. Extracted capacitance value of the wide-tuning-range tunable capacitor as a function of frequency using a series RC equivalent circuit model. The capacitance data at $V_{DC} = 5$ V is not included since it is very close to the data at $V_{DC} = 0$ V.

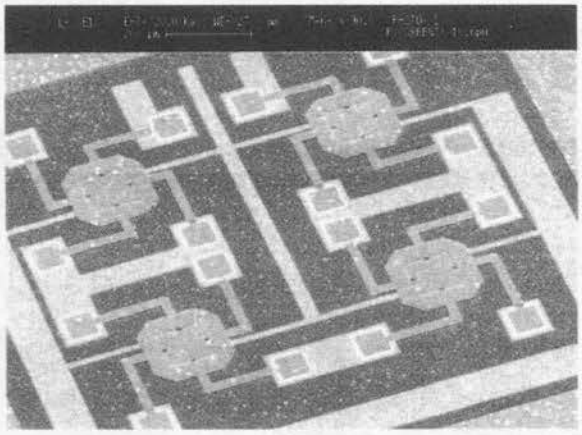

Figure 11. A scanning electron microscopic graph of an array of four wide-tuning-range tunable capacitors.

materials with even lower internal stress, which is difficult to achieve. A parallel tunable capacitor array can then be developed to increase the overall capacitance value (Fig. 11).

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BIOGRAPHIES

Jun Zou received the B.S. degree from Chongqing University, China, and the M.S. degree from Tsinghua University, China, in 1994 and 1997, respectively. He is currently a Ph.D. candidate in electrical engineering at the University of Illinois at Urbana-Champaign (UIUC). His major research interest lies in the development of novel micromachining technologies and their application to RF MEMS devices.

Chang Liu pursued his undergraduate studies at Tsinghua University, Beijing, China. He earned his M.S. and Ph.D. degrees from the California Institute of Technology in 1991 and 1996, respectively. He is currently an Assistant Professor at the University of Illinois at Urbana-Champaign, where he directs the Micro Actuators, Sensors, and Systems (MASS) research group. His group is concentrating on the following research areas: micro parallel assembly of hinged, acceleration-resistant microstructures, polymer MEMS fluidics systems, biomimetic sensors, telemetry, and investigation of microscale bubble generation. A summary of research topics being conducted at the group can be accessed from the following html web site: http://galaxy.ccsm.uiuc.edu.

José E. Schutt-Ainé received a B.S. degree from MIT in 1981, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC), in 1984 and 1988, respectively. From 1981 to 1983, he was an Application Engineer at the Hewlett-Packard Microwave Technology Center in Santa Rosa, California, where he worked on transistor modeling. During his graduate studies at UIUC, he held summer positions at GTE Network Systems in Northlake, IL. In 1989, he joined the faculty of the Electromagnetic Communication Laboratory at UIUC, where he is currently an Associate Professor of Electrical and Computer Engineering. Professor Schutt-Ainé's interests include microwave theory and measurements, electromagnetics, high-frequency circuit design, and electronic packaging.